

REMARKS/ARGUMENTS

Favorable reconsideration of this application, in light of the following discussion, is respectfully requested.

Claims 1-4 are pending in this case.

The outstanding Office Action rejected Claims 1-4 under 35 U.S.C. § 103(a) as unpatentable over Aoki (U.S. Pub. No. 2002/0044126) in view of Yoshida (U.S. Patent No. 6,670,938).

Applicants respectfully traverse the rejection of the pending claims.

The outstanding Office Action asserts that Aoki teaches every element of Claim 1 except a plurality of horizontal driving circuits, as defined by Claim 1, which it asserts Yoshida as teaching.

Specifically, the outstanding Office Action asserts, at page 4, that it would have been obvious “to combine **Aoki** teaching of a display apparatus comprising a serial-parallel converter, outputting the gradation data, wherein **each of the horizontal driving circuits including** a plurality of sampling circuits and sampling the data, and **a digital to analog converter** with **Yoshida** teaching of a plurality of horizontal driving circuits.” Emphasis of text added.

However, Aoki does not teach or suggest a horizontal driving circuit including a digital to analog converter. As depicted at Fig. 1, the D/A converter 402 of Aoki converts the signal VID', which is asserted to teach sampled gradation data as defined by Claim 1, into an analog signal before the S/P converter circuit 404 operates on it to generate VID1 to VID6, which are asserted to teach gradation data of a plurality of systems as defined by Claim 1.

Thus, Aoki, even in the proposed combination with Yoshida, fails to teach or suggest at least “a **digital to analog converter for setting levels** of output signals to the corresponding columns **based on the sampling results from said plurality of sampling**

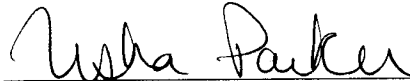
circuits,” as recited by Claim 1. Instead, the **digital to analog converter 402** of Aoki **precedes** the serial-to-parallel converter circuit 406, which generates **VID1 to VID6**, and the **sampling circuits** that operate on VID1 to VID6, such that the **D/A converter 402** of Aoki **cannot set levels “based on the sampling results from said plurality of sampling circuits,”** as recited by Claim 1.

Because Aoki and Yoshida, even in combination, do not teach or suggest at least the above-discussed features of Claim 1, Applicants respectfully request that the rejection under 35 U.S.C. § 103(a) of Claim 1 and Claims 2-4, which depend therefrom, be withdrawn.

In light of the above discussion, the present application is believed to be in condition for allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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